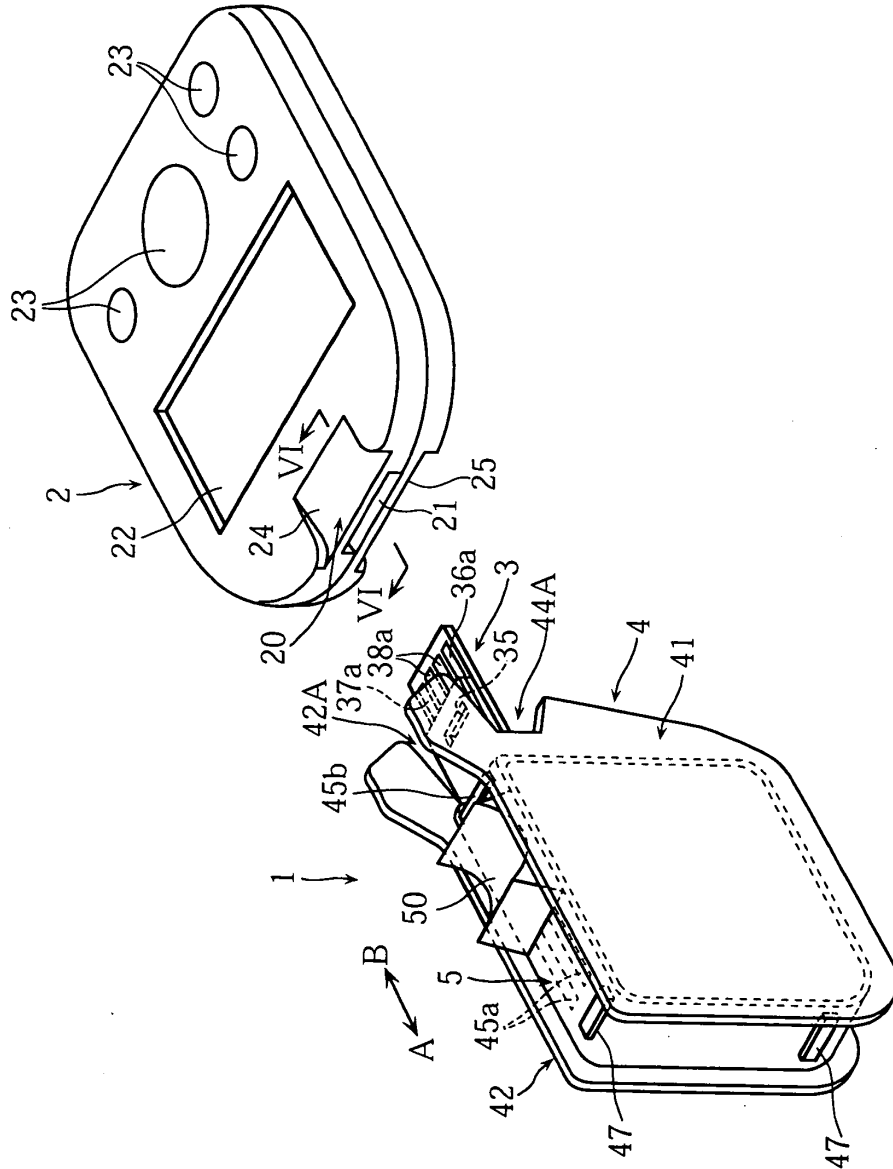


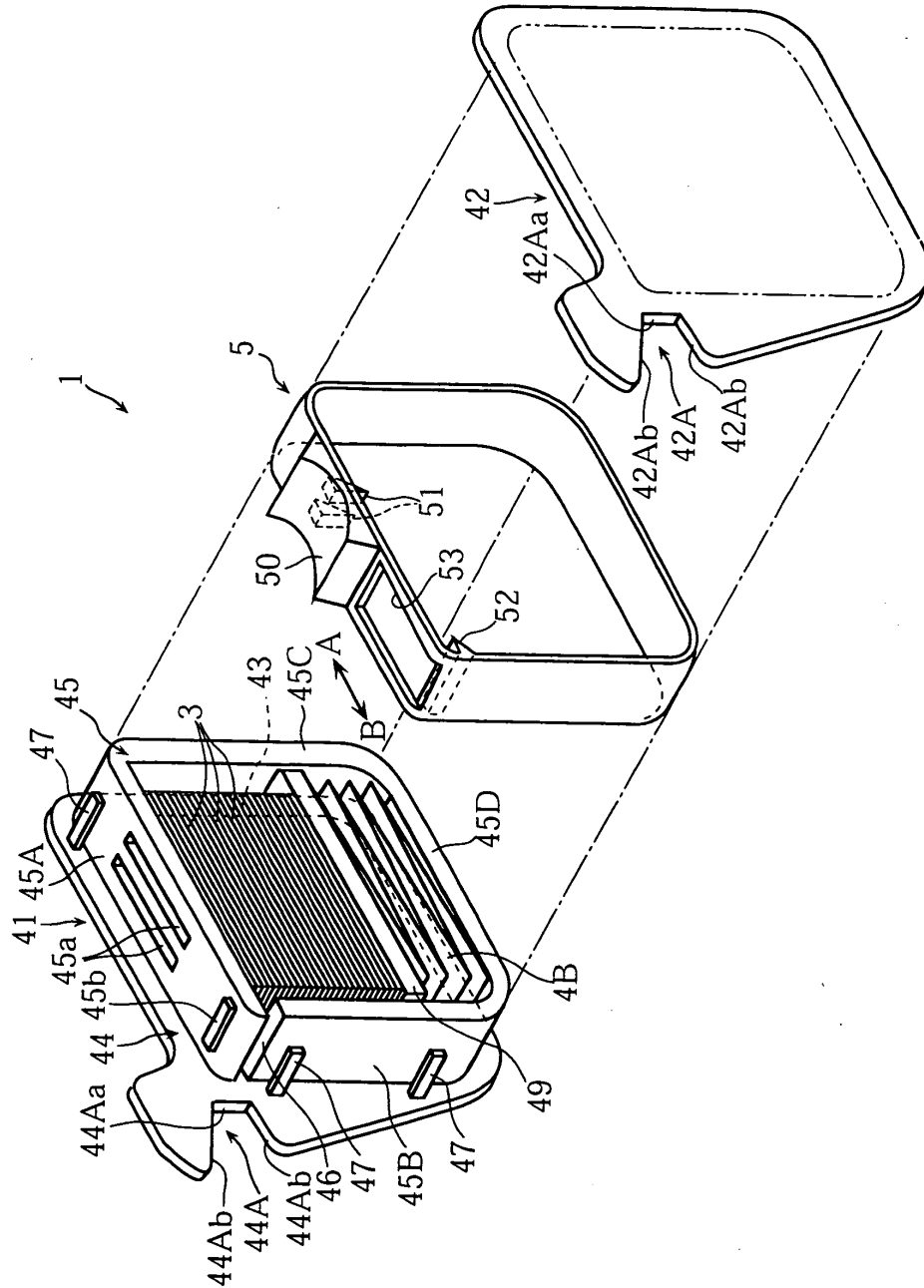
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FIG. 1



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FIG. 2



A cross-sectional view of a semiconductor device 300. The device features a substrate 30 with a base layer 31. A gate stack 32 is formed on the substrate, consisting of a gate dielectric 33 and a gate electrode 34. A source/drain region 35 is formed in the substrate, with a contact layer 36 and a contact pad 37. A passivation layer 38 is formed over the device, with a contact opening 39 exposing the contact pad 37. A conductive pad 33a is formed over the contact opening 39.

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FIG.5B

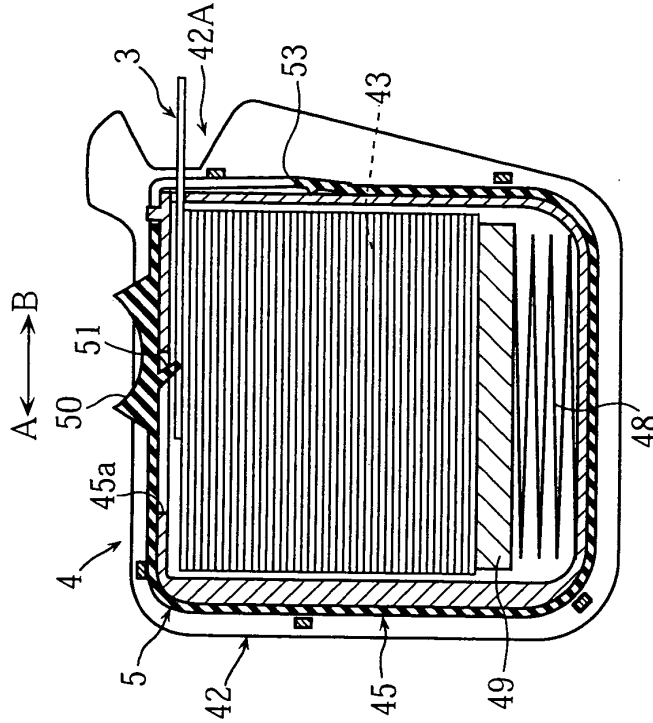
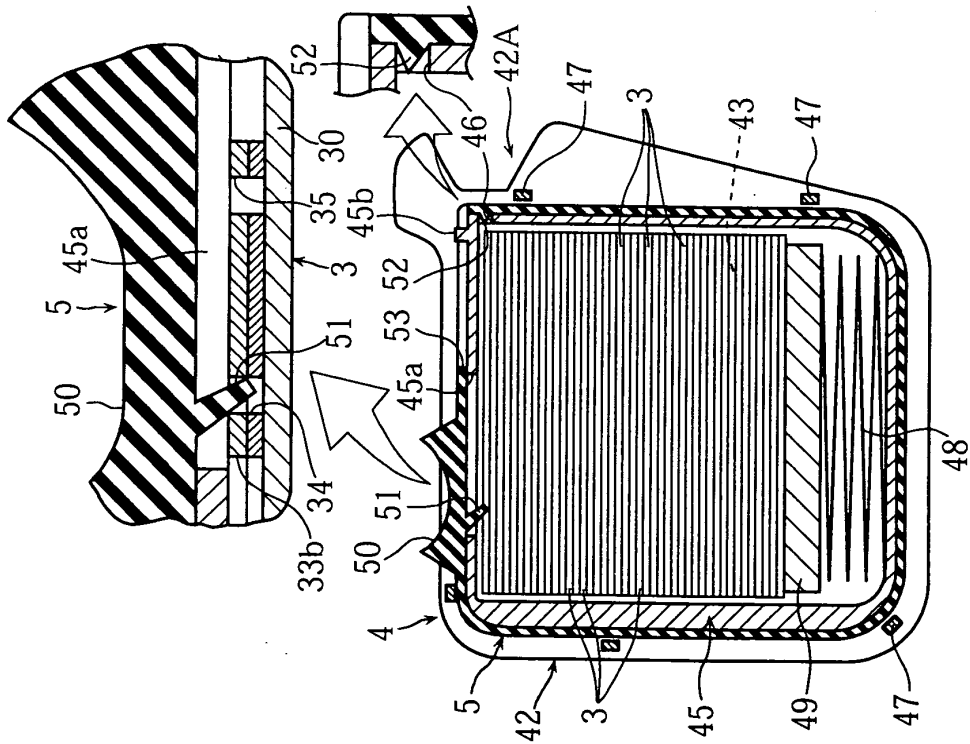
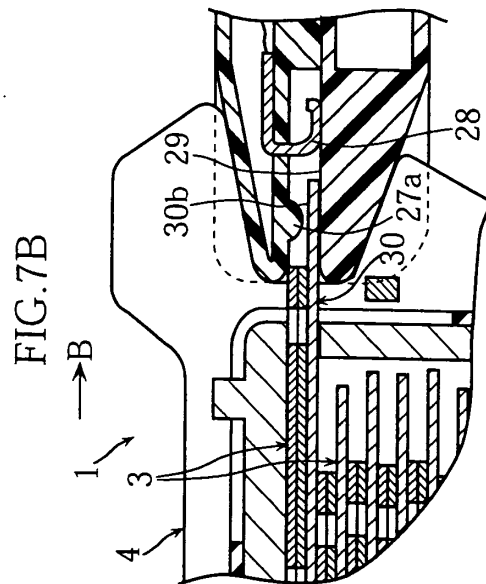
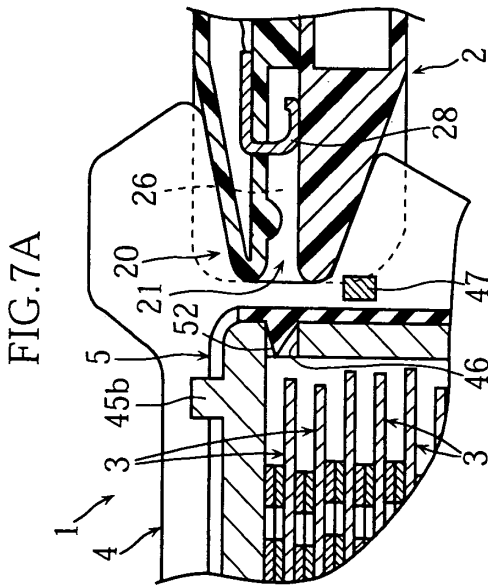
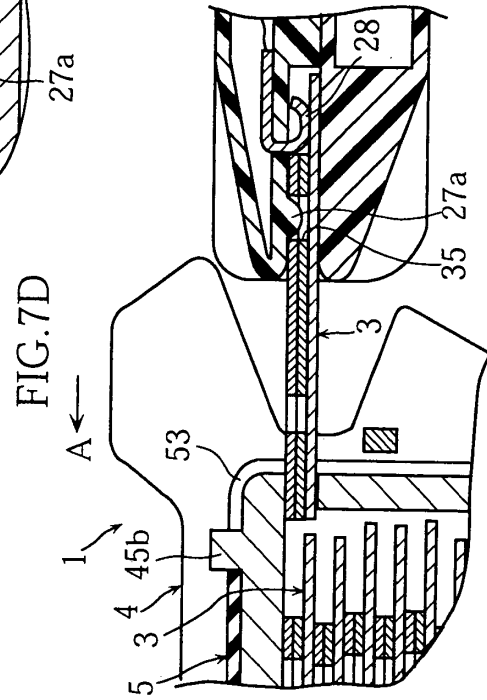
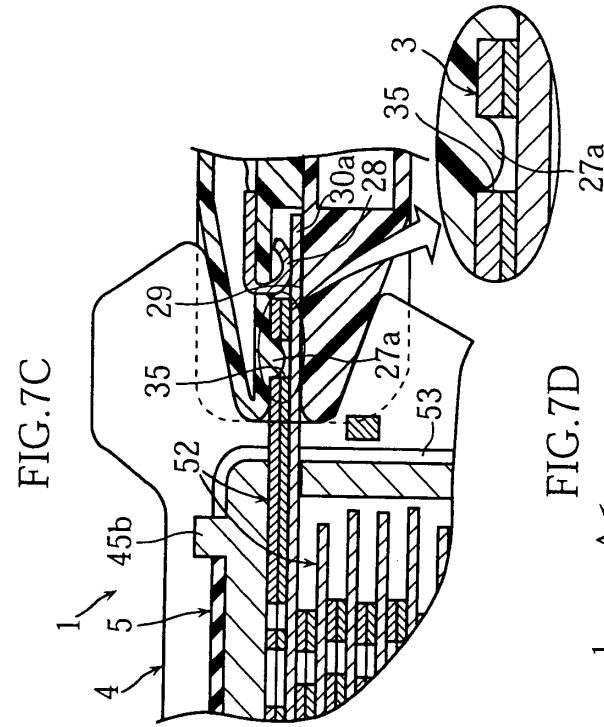


FIG.5A





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FIG.8A

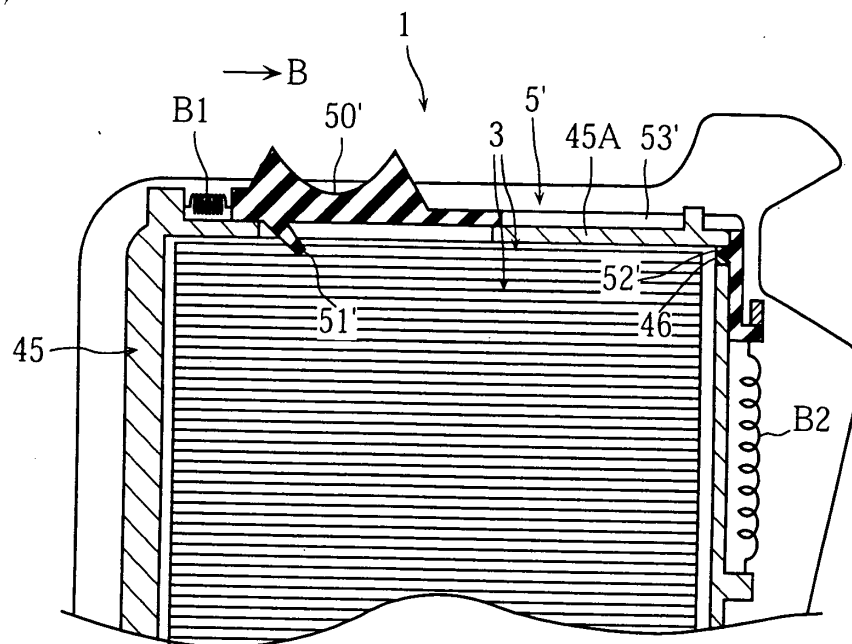
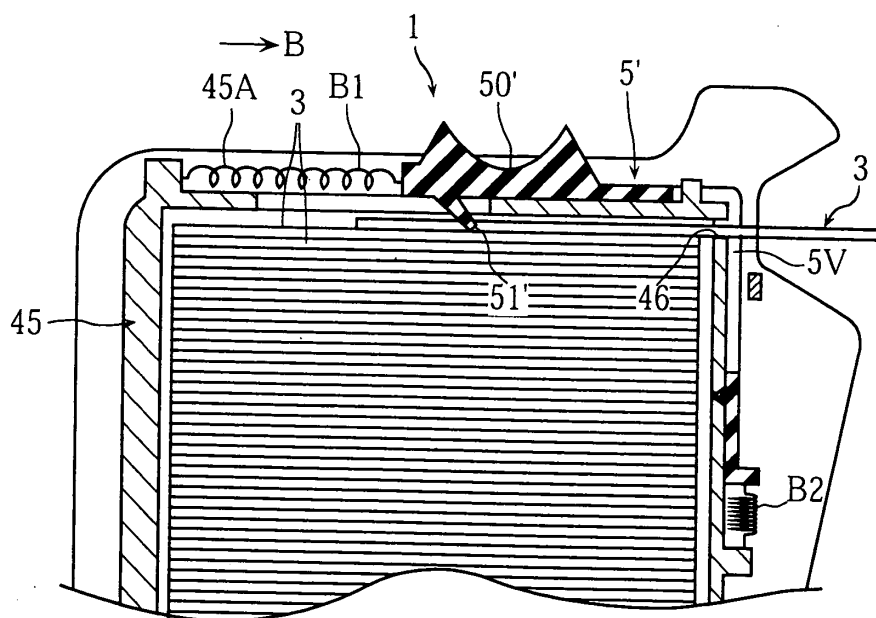


FIG.8B



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FIG.9A

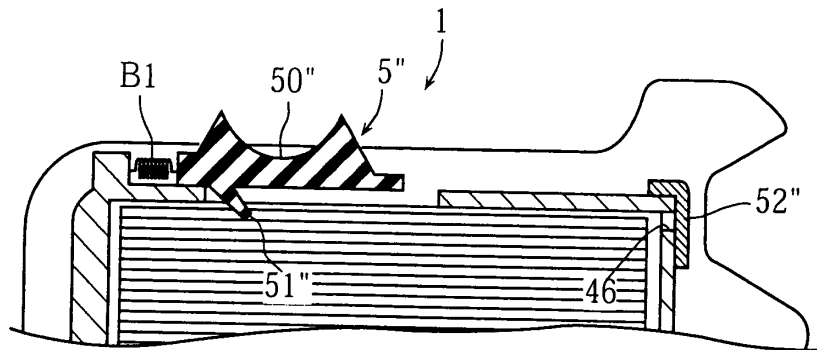
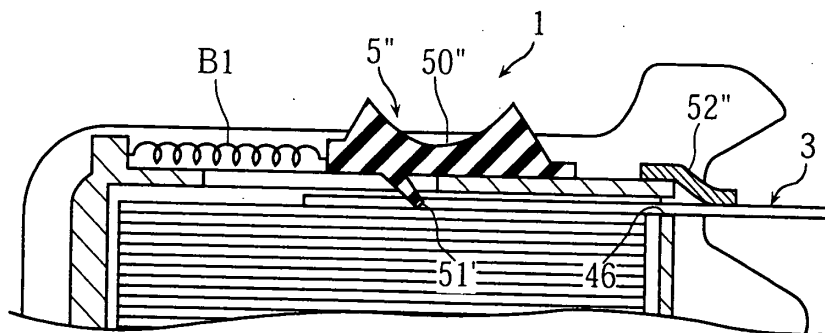


FIG.9B





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FIG.10A

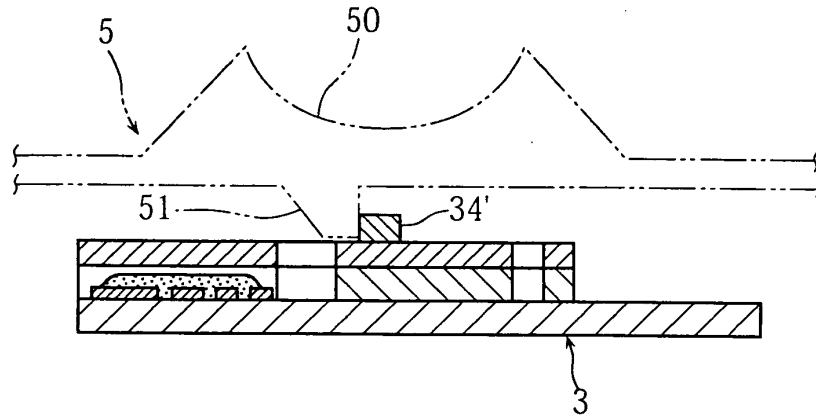


FIG.10B

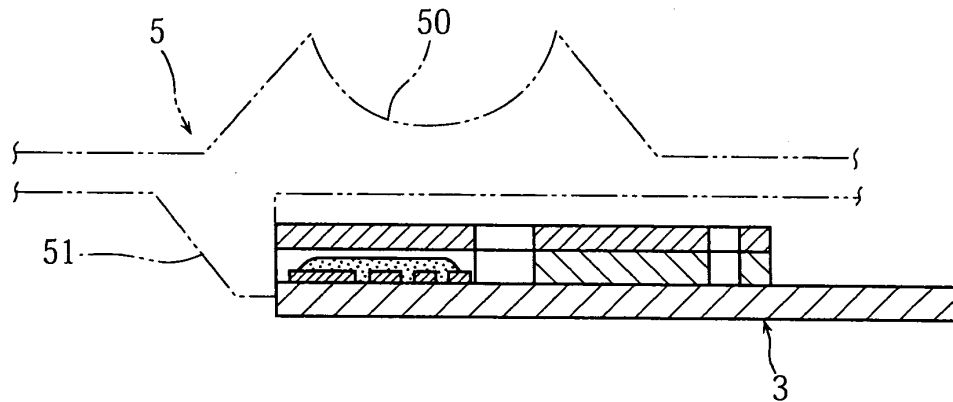
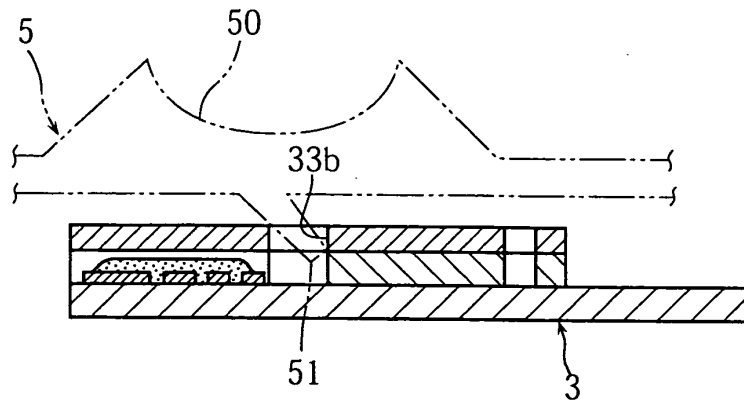


FIG.10C



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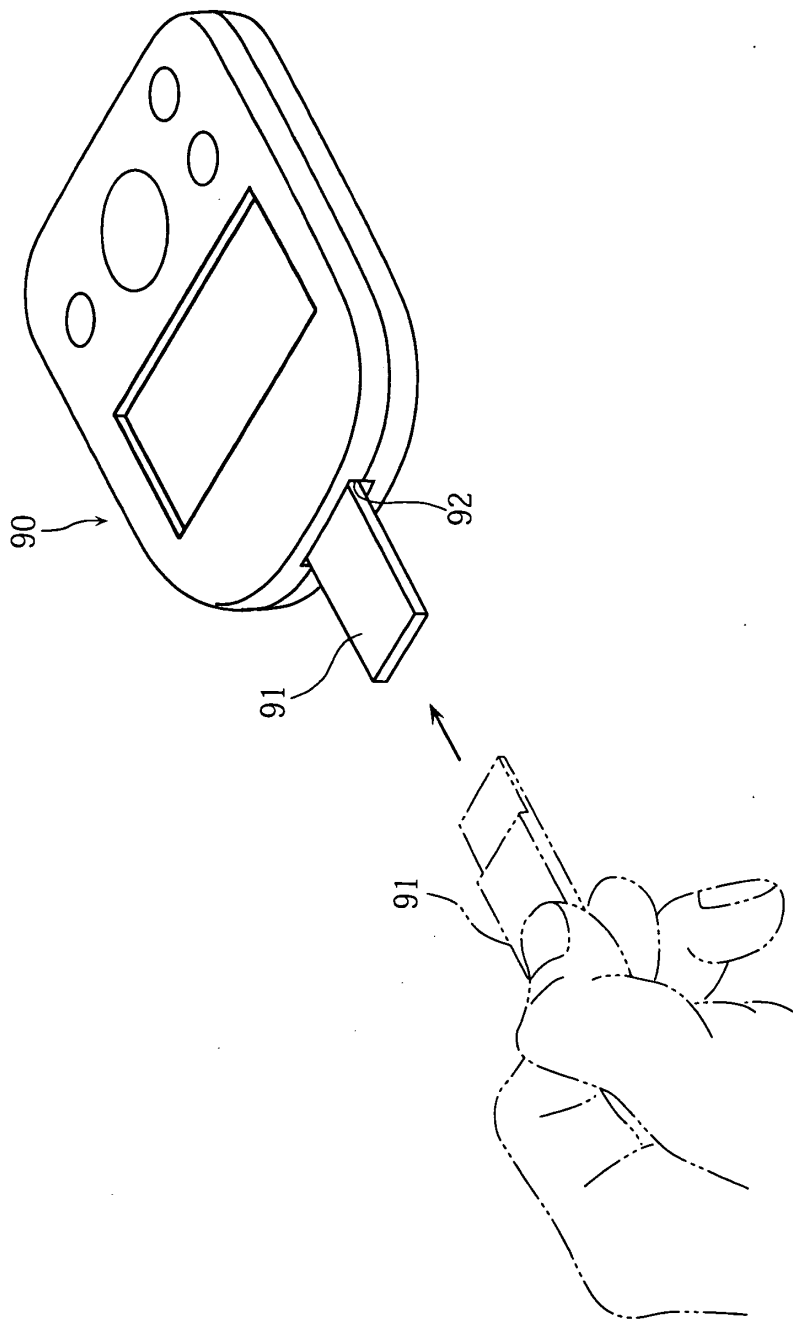


FIG. 11